

FIG. 1A

P R I O R   A R T

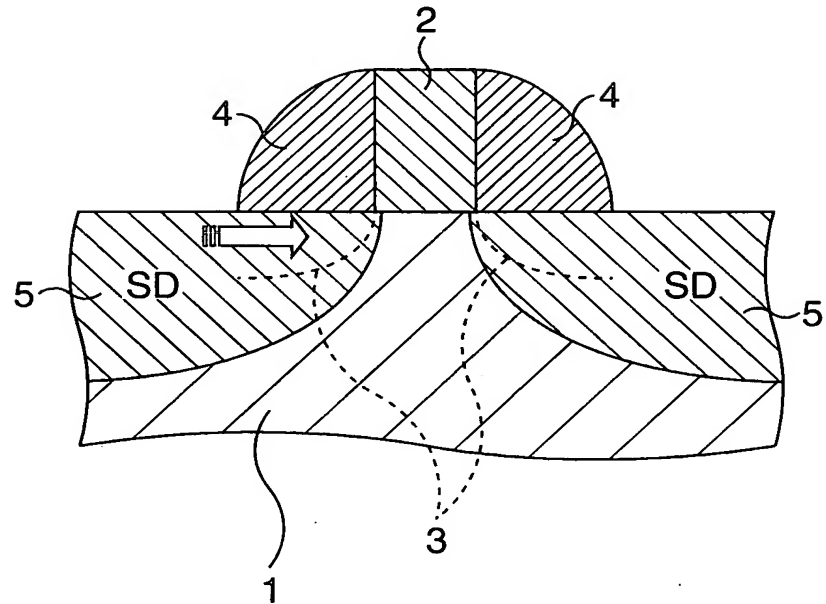


FIG. 1B

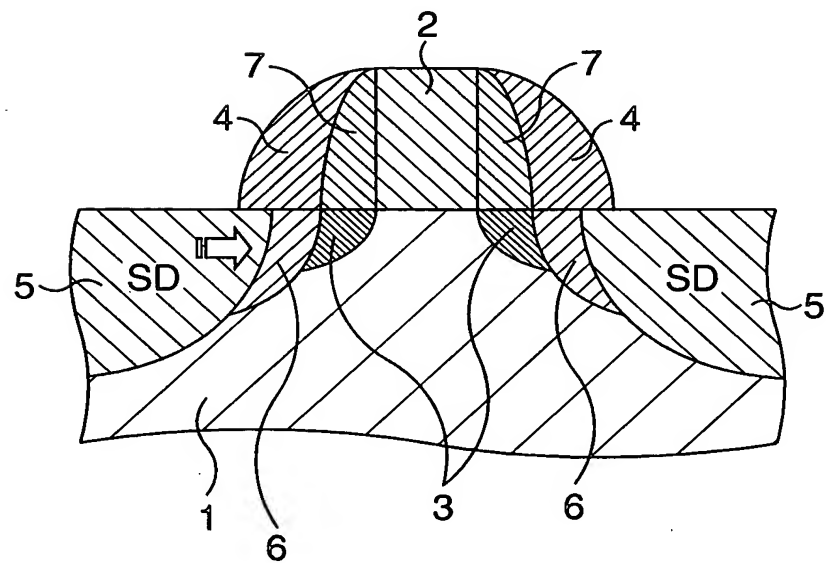


FIG. 2A

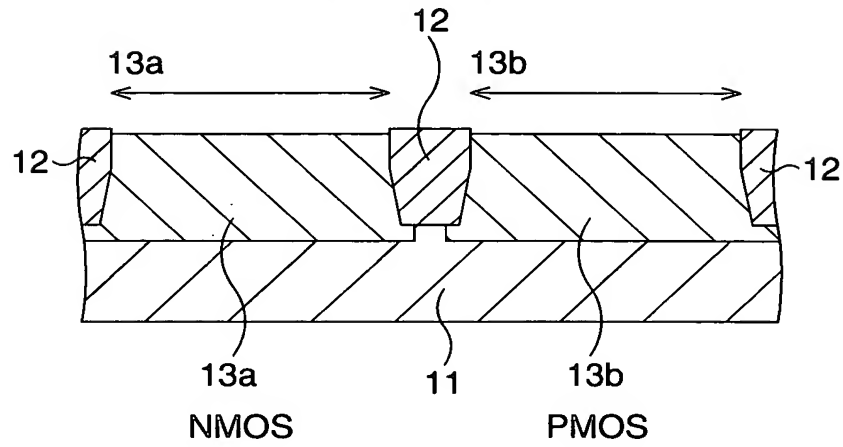


FIG. 2B

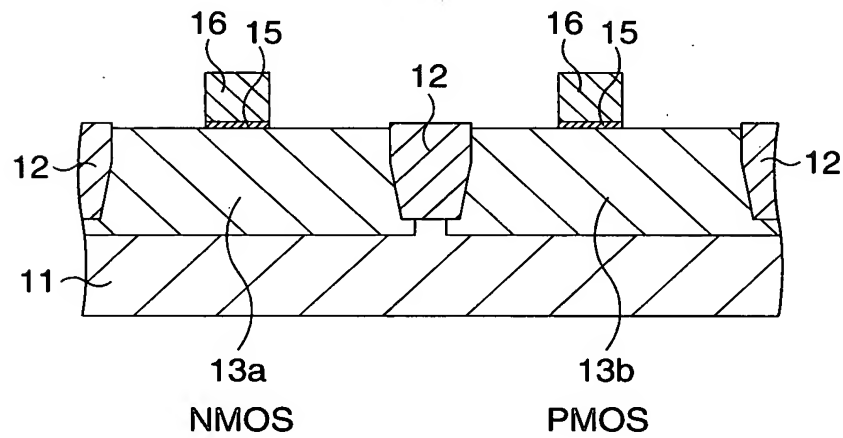
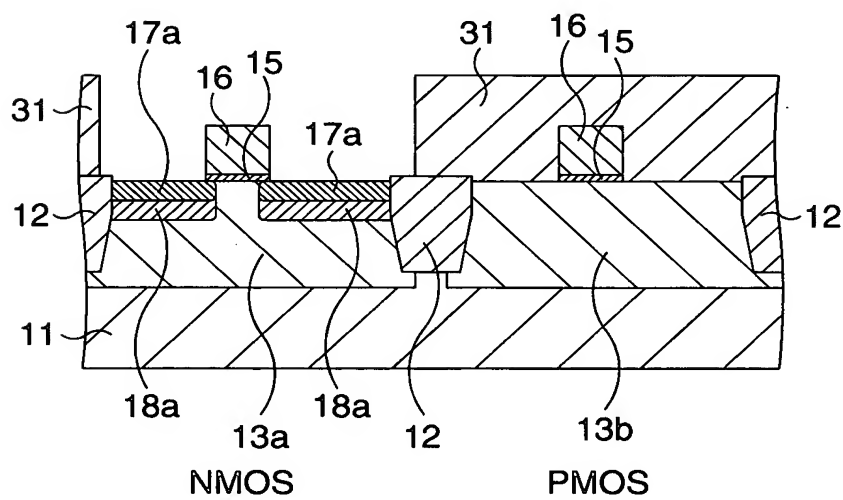


FIG. 2C





This cross-sectional view illustrates the layered structure of the semiconductor device. The substrate (11) is divided into two regions: an NMOS region on the left and a PMOS region on the right. The NMOS region contains two transistors, each with a gate stack (12, 13a) and a channel region (18a). The PMOS region contains two transistors, each with a gate stack (12, 13b) and a channel region (18b). The gate stacks are formed by a gate oxide layer (12) and a gate electrode layer (13a or 13b). The channel regions are formed by a channel oxide layer (18a or 18b) and a channel electrode layer (18b). The device is covered by a passivation layer (19) and a top layer (21). The NMOS region is also labeled with 20a and 22a, and the PMOS region with 20b and 22b. The labels 17a and 17b indicate the top surface of the gate oxide layer in the NMOS and PMOS regions, respectively. The labels 15 and 16 indicate the top surface of the channel oxide layer in the NMOS and PMOS regions, respectively. The labels 17b and 19 indicate the top surface of the gate oxide layer in the PMOS region. The labels 21 and 19 indicate the top surface of the passivation layer and the top layer, respectively.

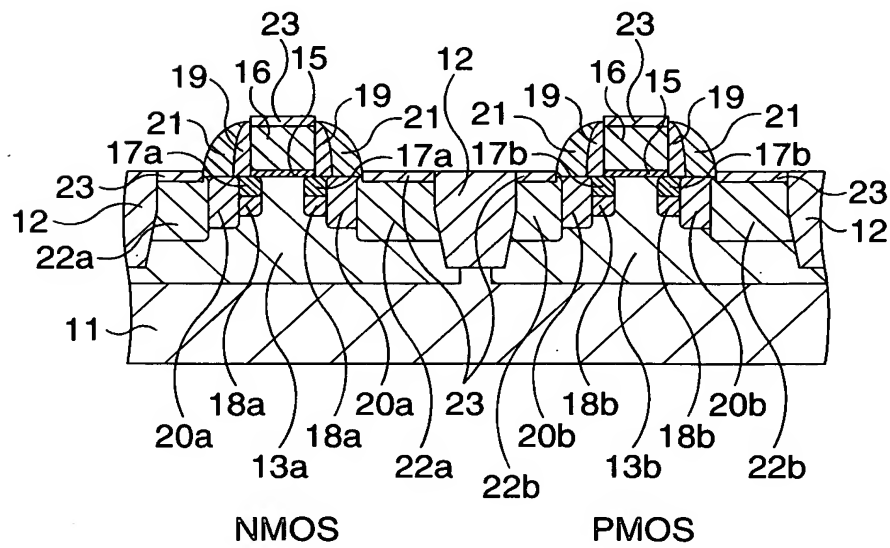


FIG. 6

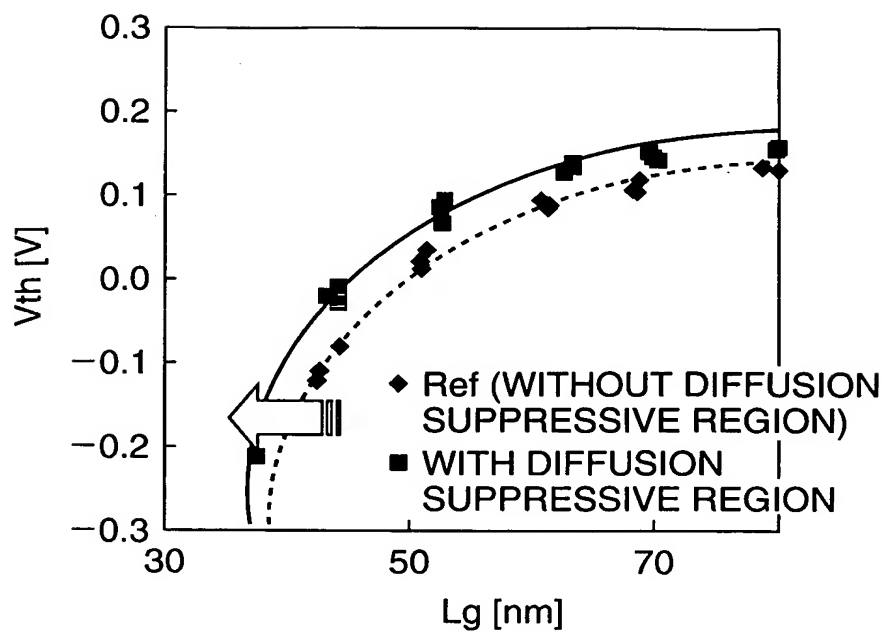


FIG. 7

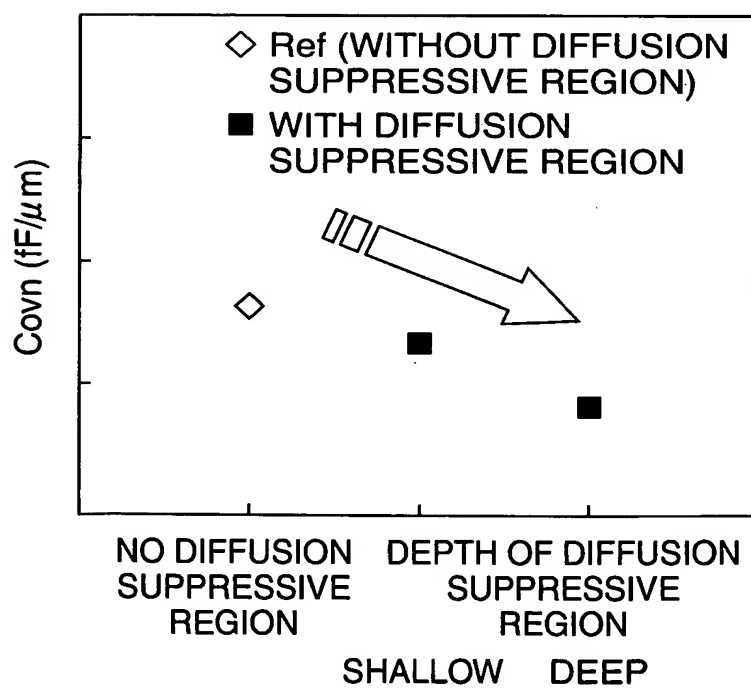


FIG. 8

